WHAT IS CLAIMED IS:

1. A sense amplifier, comprising:

cross-coupled inverters forming a latch having access lines, output nodes and conducting lines;

an enabling/disabling circuit connected between a supply terminal and a common conducting terminal of the latch;

access control transistors connected between the access lines and the output nodes of the latch;

a first equalizing circuit connected to both output nodes of the latch;

feedback means connected from the output nodes of the latch to the control terminals of the access control transistors;

a set of inverters whose outputs are connected to the conducting lines of said latch, and whose inputs a cross-connected to the output nodes of said latch, and whose conducting terminals are connected to the common conducting terminal of the latch, and

a second equalizing circuit connected to the common conducting lines of the said latch.

2. The sense amplifier as claimed in claim 1 wherein the feedback means comprises a logic gate whose inputs are connected to the output nodes and having an output connected to the control terminals of the access control transistors.

3. The sense amplifier as claimed in claim 1 wherein the enabling/disabling circuit is a MOS transistor.

4. The sense amplifier as claimed in claim 1 wherein the first and second equalizing circuits are each a pair of MOS transistors with their control terminals tied together.

5. The sense amplifier as claimed in claim 1 wherein the feedback means comprises a first inverter connected between a first output node of the latch and the control terminal of a first access control transistor and a second inverter connected between a second output node of the latch and the control terminal of a second access control transistor.

6. The sense amplifier as claimed in claim 1 wherein the feedback means comprises a NAND gate with inputs connected to the output nodes and an output connected to the control terminals of the access control transistors.

7. A sense amplifier, comprising:

a latch circuit comprised of cross-coupled latch inverters and having a first and second output;

a first access transistor coupled between the first output of the latch circuit an a first bit line;

a second access transistor coupled between the second output of the latch circuit and a second bit line; and

a feedback circuit which couples the first output of the latch circuit to a control terminal of the first access transistor and couples the second output of the latch circuit to a control terminal of the second access transistor.

8. The sense amplifier of claim 7 wherein the feedback circuit comprises:

a first inverter having an input coupled to the first output of the latch circuit and an output coupled to the control terminal of the first access transistor; and

a second inverter having an input coupled to the second output of the latch circuit and an output coupled to the control terminal of the second access transistor.

9. The sense amplifier of claim 8 further including:

a third inverter having an input coupled to the second output of the latch circuit and an output coupled to a first conducting line of a first latch inverter; and

a fourth inverter having an input coupled to the first output of the latch circuit and an output coupled to a second conducting line of a second latch inverter.

10. The sense amplifier of claim 9 further including:

a first equalizing circuit coupled between the first and second outputs of the latch circuit; and

a second equalizing circuit coupled between the first and second conducting lines.

11. The sense amplifier of claim 7 wherein the feedback circuit comprises a logic gate having inputs coupled to the first and second outputs of the latch circuit and an output coupled to the control terminals of the first and second access transistors.

12. The sense amplifier of claim 11 further including:

a fifth inverter having an input coupled to the second output of the latch circuit and an output coupled to a first conducting line of a first latch inverter; and

a sixth inverter having an input coupled to the first output of the latch circuit and an output coupled to a second conducting line of a second latch inverter.

13. The sense amplifier of claim 12 further including:

a first equalizing circuit coupled between the first and second outputs of the latch circuit; and

a second equalizing circuit coupled between the first and second conducting lines.

14. The sense amplifier of claim 11 wherein the logic gate is a NAND gate.

15. A sense amplifier, comprising:

a latch circuit comprised of cross-coupled first and second latch inverters and having a first and second output;

a first inverter having an input coupled to the second output of the latch circuit and an output coupled to a first conducting line of the first latch inverter; and

a second inverter having an input coupled to the first output of the latch circuit and an output coupled to a second conducting line of the second latch inverter.

16. The sense amplifier of claim 15 further including:

a first equalizing circuit coupled between the first and second outputs of the latch circuit; and

a second equalizing circuit coupled between the first and second conducting lines.

17. The sense amplifier of claim 15 further including:

a first access transistor coupled between the first output of the latch circuit an a first bit line;

a second access transistor coupled between the second output of the latch circuit and a second bit line; and

a feedback circuit which couples the first output of the latch circuit to a control terminal of the first access transistor and couples the second output of the latch circuit to a control terminal of the second access transistor.

18. The sense amplifier of claim 17 wherein the feedback circuit comprises:

a third inverter having an input coupled to the first output of the latch circuit and an output coupled to the control terminal of the first access transistor; and

a fourth inverter having an input coupled to the second output of the latch circuit and an output coupled to the control terminal of the second access transistor.

19. The sense amplifier of claim 17 wherein the feedback circuit comprises a logic gate having inputs coupled to the first and second outputs of the latch circuit and an output coupled to the control terminals of the first and second access transistors.

20. The sense amplifier of claim 19 wherein the logic gate is a NAND gate.